

AC7926A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version 1.3

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Revision History

Date	Revision	Author	Description
2024.05.30	V1.0	zh-jieli	Initial Release
2024.09.30	V1.1	zh-jieli	Modify Package Information, Add Power Domain Information
2024.12.07	V1.2	zh-jieli	Modify Audio DAC Characteristics, IO Characteristics and Operating Temperature
2025.01.09	V1.3	zh-jieli	Update Feature_Bluetooth, Update Block Diagram

Table of Contents

Revision History	1
Table of Contents	2
AC7926A Features	3
1 Block Diagram	5
2 Pin Definition	6
2.1 Pin Assignment	6
2.2 Pin Description	7
3 Electrical Characteristics	16
3.1 Absolute Maximum Ratings	16
3.2 ESD Ratings	16
3.3 PMU Characteristics	16
3.4 IO Characteristics	17
3.5 Audio DAC Characteristics	20
3.6 Audio ADC Characteristics	21
3.7 BT Characteristics	22
3.8 WiFi Characteristics	22
4 Package Information	24
4.1 QFN132_10*10mm	24
5 IC Marking Information	25
6 Solder-Reflow Condition	26

AC7926A Features

SYSTEM

- Dual Core 32bit DSP 320MHz
- With IEEE754 Single precision FPU
- Support jieli TEE
- Support FFT / MATRIX / MATH
- 2 x I-cache and D-cache
- On-chip SRAM 352kbyte
- Support SDTAP / EMU / ETM
- Support MMU
- Support MPU
- Built-in SDRAM/DDR (Maximum 64Mbyte)
- SPI FLASH Controller (Maximum 64Mbyte)
- 24MHz crystal oscillator
- 32KHz RTC crystal oscillator
- Internal RC oscillator, PLL

Video Input

- Internal Image Signal Processor
- Support DVP, BT656, SPI interface
- Support 1 lane MIPI-CSI interface
- Support RAW, YUV422 formats
- Support video resize an time mark
- 2 x JPEG codec

Video output

- Support display color enhancement
- Support DPI, DBI, BT656 interface
- Support 4 lane MIPI-DSI interface
- Support RGB, YUV formats

Graphics

- Internal 2D DMA
- Internal 2.5D GPU
- Support vector graphics rendering
- Support image resize, rotation, projection
- Support multiple blending mode
- Support ARGB, RGB, YUV, Lx, Ax formats

DSP Audio Processing

- SBC/AAC/LDAC/LHDC/LC3/CVSD/mSBC codec
- mSBC voice codec supported for BT phone
- PLC for voice processing
- Single/Multi MIC ENC
- Multi-band DRC
- Multi-band EQ
- Support spatial sound

Audio

- 2 x 16bit DAC
 - ❖ SNR 103dB
 - ❖ Noise 6.4uVrms
 - ❖ Supports differential mode
 - ❖ Sampling rate 8~96kHz
- 2 x 16bit ADC
 - ❖ SNR 95dB
 - ❖ Sampling rate 8~48kHz
- I2S/PDM AUDIO Master/Slave interface

Bluetooth

- Dual-mode BT6.0 with LE Audio (DN Q332415)
- Support AoA/AoD
- Support LE audio BIS/CIS
- Support long range BLE
- Maximum transmitting power 19 dBm
- Receiver sensitivity
 - ❖ -95.5 dBm @BR
 - ❖ -96 dBm @EDR $\pi/4$ DQPSK
 - ❖ -88 dBm @EDR 8DPSK

IEEE 802.11b/g/n

- 1T1R in 2.4 GHz band
- 20 MHz and 40 MHz bandwidth
- Data rate up to 150 Mbps
- Security: WFA/WPA3 personal, WPS2.0, WAPI
- QoS: WFA WMM, WMM PS
- Support STBC, A-MPDU, A-MSDU, BLK-ACK
- Support Station, SoftAP, Station+SoftAP, Promiscuous mode
- Maximum transmitting power
 - ❖ 19 dBm @1Mbps, DSSS
 - ❖ 17 dBm @HT20, MCS0
 - ❖ 13 dBm @HT20, MCS7
- Receiver sensitivity
 - ❖ -97 dBm @1Mbps, DSSS
 - ❖ -93 dBm @HT20, MCS0
 - ❖ -74 dBm @HT20, MCS7

Peripherals

- 1 x High speed USB
- 1 x Full speed USB
- 2 x SD host controller
- 6 x Multi-function 32bit timer
- 5 x UART interface
- 3 x I²C Master/Slave interface
- 3 x SPI Master/Slave interface
- 1 x QDEC
- 1 x CAN Controller
- 1 x Ethernet Mac
- 8 x MCPWM
- 1 x PAP Interface
- 3 x Light strip Controller
- 1 x 10bit ADC(16 Channel)
- 77 x GPIO Support function remapping
- Built-in RTC with alarm, wakeup

PMU

- 1 x Buck DC-DC converter
- 3 x IO power domain
- WIFI PA support external power supply
- RTCVDD33 support external power supply
- Support temperature sensor
- VBAT range 2.7V to 5.5V
- IOVDD range 2.7V to 3.6V

Packages

- QFN132(10mm*10mm)

Temperature

- Operating temperature
TC = -20°C to +85°C (standard range)
- Storage temperature -65°C to +150°C

Applications

- IPC
- Driving recorder
- WIFI Appliances

1 Block Diagram

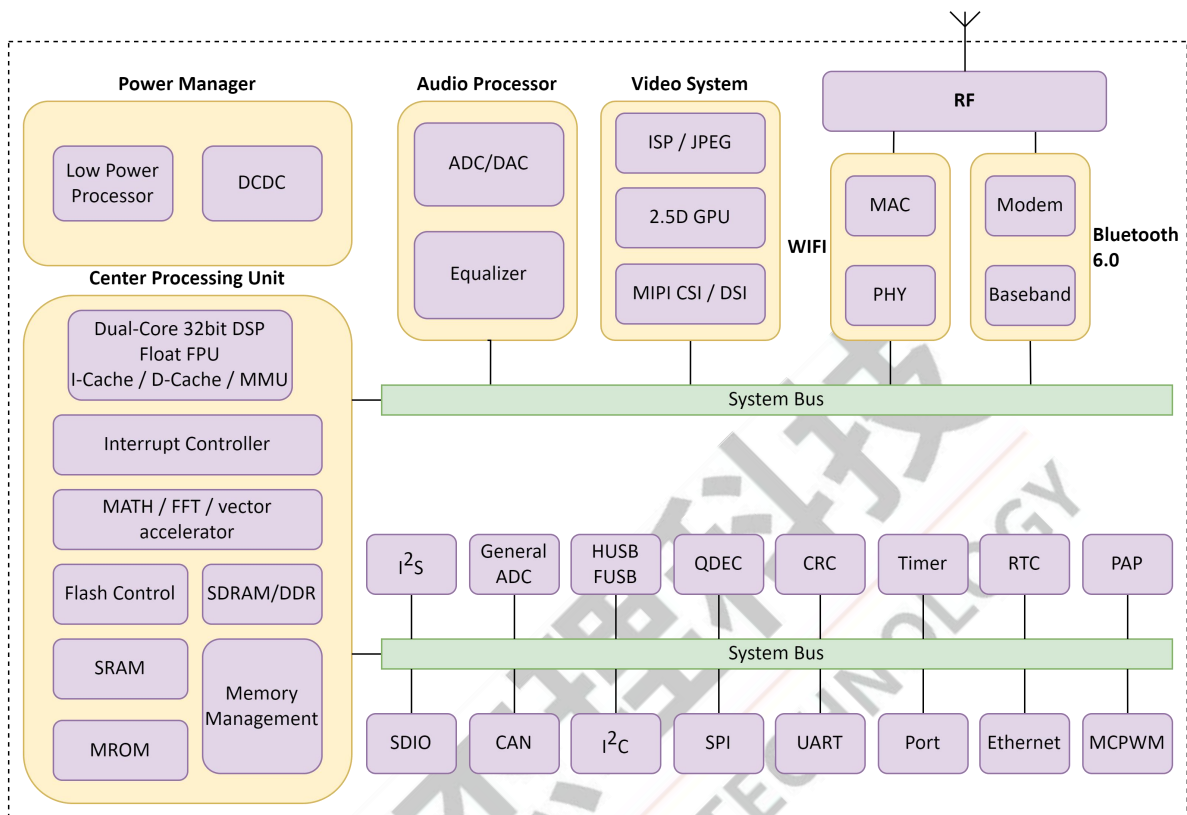


Figure 1-1 AC7926A Block Diagram

2 Pin Definition

2.1 Pin Assignment

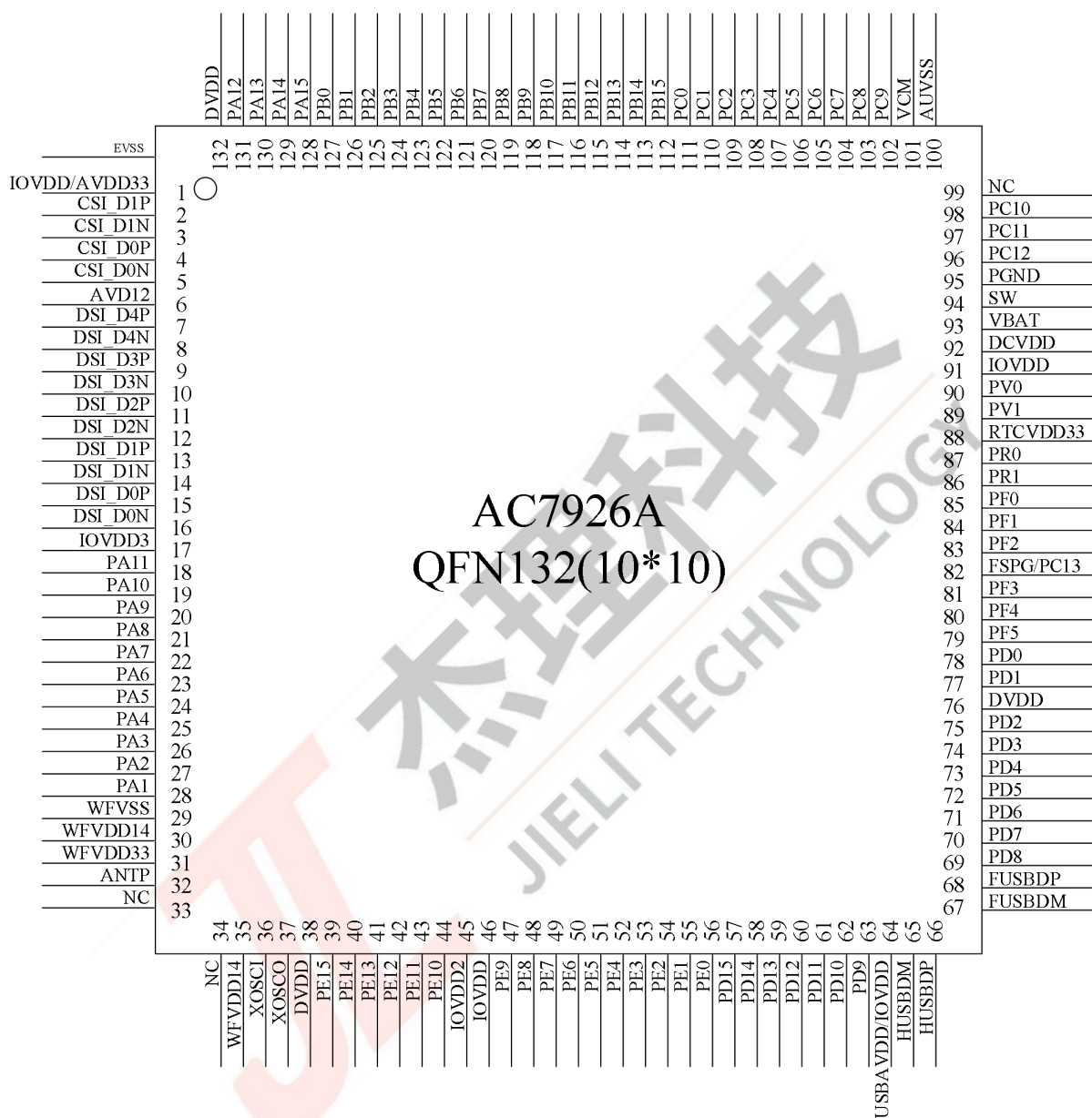


Figure 2-1 AC7926A Pin Assignment

2.2 Pin Description

Table 2-2-1 AC7926A Pin Description

Pin No.	Name	Type	IO Initial State	Description
1	IOVDD	P	--	IO Power
	AVD33	P	--	Analog 3.3V Power
2	CSI_D1P	I	--	MIPI CSI D1P
3	CSI_D1N	I	--	MIPI CSI D1N
4	CSI_D0P	I	--	MIPI CSI D0P
5	CSI_D0N	I	--	MIPI CSI D0N
6	AVD12	P	--	Analog 1.2V Power
7	DSI_D4P	I/O	--	MIPI DSI D4P
8	DSI_D4N	I/O	--	MIPI DSI D4N
9	DSI_D3P	I/O	--	MIPI DSI D3P
10	DSI_D3N	I/O	--	MIPI DSI D3N
11	DSI_D2P	I/O	--	MIPI DSI D2P
12	DSI_D2N	I/O	--	MIPI DSI D2N
13	DSI_D1P	I/O	--	MIPI DSI D1P
14	DSI_D1N	I/O	--	MIPI DSI D1N
15	DSI_D0P	I/O	--	MIPI DSI D0P
16	DSI_D0N	I/O	--	MIPI DSI D0N
17	IOVDD3	P	--	IO Power for PA1~PA11
18	PA11	I/O	Z	LCD_DATA7(A) Sensor0_D9(B) PAP_D7(A) TS0_DATA5
19	PA10	I/O	Z	SFC1_DO LCD_DATA6(A) Sensor0_D8(B) PAP_D6(A) TS0_DATA4 SD0_DATA3(B)
20	PA9	I/O	Z	SFC1_CLK LCD_DATA5(A) Sensor0_D7(B) PAP_D5(A) TS0_DATA3 SD0_DATA2(B)

Pin No.	Name	Type	IO Initial State	Description
21	PA8	I/O	Z	SFC1_DATA3 LCD_DATA4(A) Sensor0_D6(B) PAP_D4(A) TS0_DATA2 SD0_DATA1(B)
22	PA7	I/O	Z	LCD_DATA3(A) Sensor0_D5(B) PAP_D3(A) TS0_DATA1 SD0_CLK(B)
23	PA6	I/O	Z	SFC1_DATA2 LCD_DATA2(A) Sensor0_D4(B) PAP_D2(A) TS0_DATA0 SD0_CMD(B)
24	PA5	I/O	Z	SFC1_DI LCD_DATA1(A) Sensor0_D3(B) PAP_D1(A) TS0_CLK SD0_DATA0(B)
25	PA4	I/O	Z	SFC1_CS LCD_DATA0(A) Sensor0_D2(B) PAP_D0(A) TS0_SYNC
26	PA3	I/O	Z	Sensor0_CLK(B) TS0_VALID
27	PA2	I/O	Z	Sensor0_SYNC1(B) TS0_ERROR
28	PA1	I/O	Z	Sensor0_SYNC0(B)
29	WVSS	G	--	Ground of Wireless
30	WVDD14	P	--	Wireless 1.4V Power
31	WVDD33	P	--	Wireless 3.3V Power
32	ANTP	RF	--	Antenna Positive Port
33	NC	--	--	--
34	NC	--	--	--
35	WVDD14	P	--	Wireless 1.4V Power
36	XOSCI	I	--	Crystal Oscillator Input

Pin No.	Name	Type	IO Initial State	Description
37	XOSCO	O	--	Crystal Oscillator Output
38	DVDD	P	--	Digital Logic Power
39	PE15	I/O	Z	--
40	PE14	I/O	Z	--
41	PE13	I/O	Z	--
42	PE12	I/O	Z	--
43	PE11	I/O	Z	--
44	PE10	I/O	Z	--
45	IOVDD2	P	--	IO Power for PE10~PE15
46	IOVDD	P	--	IO Power for PA12~PA15, PB0~PB15, PC0~PC13, PD0~PD15, PE0~PE9, PF0~PF5, PV0~PV1
47	PE9	I/O	Z	ADC12(ADC Input Channel 12) IO Wakeup Channel 12 SD0_DATA3(C)
48	PE8	I/O	Z	ADC11(ADC Input Channel 11) IO Wakeup Channel 11 SD0_DATA2(C) Ethnet MII_COL
49	PE7	I/O	Z	ADC10(ADC Input Channel 10) IO Wakeup Channel 10 SD0_DATA1(C) Ethnet MII_TXERR
50	PE6	I/O	Z	ADC9(ADC Input Channel 9) IO Wakeup Channel 9 SD0_CLK(C) Ethnet MII_RXDV
51	PE5	I/O	Z	ADC8(ADC Input Channel 8) IO Wakeup Channel 8 SD0_CMD(C) Ethnet MII_RXCK Sensor0_SYNC1(A)
52	PE4	I/O	Z	ADC7(ADC Input Channel 7) IO Wakeup Channel 7 SD0_DATA0(C) Ethnet MII_RX3 Sensor0_SYNC0(A)
53	PE3	I/O	Z	SensorX_CLK Sensor0_CLK(A) Ethnet MII_RX2

Pin No.	Name	Type	IO Initial State	Description
54	PE2	I/O	Z	SensorX_D7 Sensor0_D9(A) Ethnet MII_RX1 Ethnet RMII_RX1(A)
55	PE1	I/O	Z	SensorX_D6 Sensor0_D8(A) Ethnet MII_RX0 Ethnet RMII_RX0(A)
56	PE0	I/O	Z	SensorX_D5 Sensor0_D7(A) Ethnet MII_CRS Ethnet RMII_CRSDV(A) SD1_CLK(B)
57	PD15	I/O	Z	SensorX_D4 Sensor0_D6(A) Ethnet MII_TXCK Ethnet RMII_REFCLK(A) SD1_CMD(B)
58	PD14	I/O	Z	SensorX_D3 Sensor0_D5(A) Ethnet MII_RXERR Ethnet RMII_RXERR(A) SD1_DATA0(B)
59	PD13	I/O	Z	SensorX_D2 Sensor0_D4(A) Ethnet MII_TXEN Ethnet RMII_TXEN(A) SD1_DATA1(B)
60	PD12	I/O	Z	SensorX_D1 Sensor0_D3(A) Ethnet MII_TX1 Ethnet RMII_TX1(A) SD1_DATA2(B)
61	PD11	I/O	Z	SensorX_D0 Sensor0_D2(A) Ethnet MII_TX0 Ethnet RMII_TX0(A) SD1_DATA3(B)

Pin No.	Name	Type	IO Initial State	Description
62	PD10	I/O	Z	ADC6(ADC Input Channel 6) IO Wakeup Channel 6 Sensor0_D1(A) Ethnet MII_TX3
63	PD9	I/O	Z	ADC5(ADC Input Channel 5) IO Wakeup Channel 5 Sensor0_D0(A) Ethnet MII_TX2
64	USBAVDD	P	--	High Speed USB Power
	IOVDD	P	--	IO Power
65	HUSBDM	I/O	15kΩ Pull-down	High Speed USB Negative Data
66	HUSBDP	I/O	15kΩ Pull-down	High Speed USB Positive Data
67	FUSBDM	I/O	15kΩ Pull-down	Full Speed USB Negative Data ADC15(ADC Input Channel 15) IO Wakeup Channel 15
68	FUSBDP	I/O	15kΩ Pull-down	Full Speed USB Positive Data ADC14(ADC Input Channel 14) IO Wakeup Channel 14
69	PD8	I/O	10kΩ Pull-up	MCLR(Device Reset) ADC4(ADC Input Channel 4) SD Power IO Wakeup Channel 4
70	PD7	I/O	Z	ADC3(ADC Input Channel 3) IO Wakeup Channel 3 SD0_CLK(A)
71	PD6	I/O	Z	ADC2(ADC Input Channel 2) IO Wakeup Channel 2 SD0_CMD(A)
72	PD5	I/O	Z	SD0_DATA0(A)
73	PD4	I/O	Z	SD0_DATA1(A)
74	PD3	I/O	Z	SD0_DATA2(A)
75	PD2	I/O	Z	SD0_DATA3(A)
76	DVDD	P	--	Digital Logic Power
77	PD1	I/O	10kΩ Pull-up	Hold down 0 to reset ADC1(ADC Input Channel 1) IO Wakeup Channel 1
78	PD0	I/O	Z	ADC0(ADC Input Channel 0) IO Wakeup Channel 0
79	PF5	I/O	Z	SFCTZ_DO SPITZ_DO

Pin No.	Name	Type	IO Initial State	Description
80	PF4	I/O	Z	SFCTZ_CLK SPITZ_CLK
81	PF3	I/O	Z	SFCTZ_DATA3 SPITZ_DATA3
82	FSPG	I/O	Z	Flash Power Output
	PC13	I/O	Z	ADC13(ADC Input Channel 13) IO Wakeup Channel 13
83	PF2	I/O	Z	SFCTZ_DATA2 SPITZ_DATA2
84	PF1	I/O	Z	SFCTZ_DI SPITZ_DI
85	PF0	I/O	Z	SFCTZ_CS SPITZ_CS
86	PR1	I/O	Z	32k Crystal Oscillator Output
87	PR0	I/O	Z	32k Crystal Oscillator Input
88	RTCVDD33	P	--	RTC Power for PR0~PR1
89	PV1	I/O	Z	AVDD18
90	PV0	I/O	Z	AVDD28
91	IOVDD	P	--	IO Power
92	DCVDD	P	--	DCDC Power
93	VBAT	P	--	Battery Input
94	SW	P	--	Buck DCDC Switch Port
95	PGND	G	--	Ground of Buck DC-DC converter
96	PC12	I/O	Z	AIN_BN0(Audio ADC Negative Input)
97	PC11	I/O	Z	AIN_BP0(Audio ADC Positive Input)
98	PC10	I/O	10kΩ Pull-down	LVD(External Low Voltage Detection Input) MICBIASB (MIC Bias Output)
99	NC	--	--	--
100	AUVSS	G	--	Audio Ground
101	VCM	P	--	Audio Reference Power
102	PC9	I/O	Z	MICBIASA (MIC Bias Output) Right Channel DAC Output
103	PC8	I/O	Z	Left Channel DAC Output
104	PC7	I/O	Z	AIN_AP0(Audio ADC Positive Input)
105	PC6	I/O	Z	AIN_AN0(Audio ADC Negative Input)
106	PC5	I/O	Z	AIN_BN1(Audio ADC Negative Input)
107	PC4	I/O	Z	AIN_BP1(Audio ADC Positive Input)
108	PC3	I/O	Z	AIN_AP1(Audio ADC Positive Input)
109	PC2	I/O	Z	AIN_AN1(Audio ADC Negative Input) Sensor1_SYNC1(B)

Pin No.	Name	Type	IO Initial State	Description
110	PC1	I/O	Z	Sensor1_SYNC0(B) LCD_DATA7(B) PAP_D7(B)
111	PC0	I/O	Z	Sensor1_CLK(B) LCD_DATA6(B) PAP_D6(B)
112	PB15	I/O	Z	LCD_DATA23(A) Sensor1_D7(B) LCD_DATA5(B) PAP_D5(B) SD1_CLK(A)
113	PB14	I/O	Z	LCD_DATA22(A) Sensor1_D6(B) LCD_DATA4(B) PAP_D4(B) SD1_CMD(A)
114	PB13	I/O	Z	LCD_DATA21(A) Sensor1_D5(B) LCD_DATA3(B) PAP_D3(B) SD1_DATA0(A)
115	PB12	I/O	Z	LCD_DATA20(A) Sensor1_D4(B) LCD_DATA2(B) PAP_D2(B) SD1_DATA1(A)
116	PB11	I/O	Z	LCD_DATA19(A) Sensor1_D3(B) LCD_DATA1(B) PAP_D1(B) SD1_DATA2(A) TS1_DATA7
117	PB10	I/O	Z	LCD_DATA18(A) Sensor1_D2(B) LCD_DATA0(B) PAP_D0(B) SD1_DATA3(A) TS1_DATA6
118	PB9	I/O	Z	LCD_DATA17(A/B) Sensor1_D1(B) TS1_DATA5

Pin No.	Name	Type	IO Initial State	Description
119	PB8	I/O	Z	LCD_DATA16(A/B) Sensor1_D0(B) TS1_DATA4
120	PB7	I/O	Z	LCD_DATA15(A/B) Sensor1_D7(A) PAP_D15(A/B) TS1_DATA3 SD0_CLK(D)
121	PB6	I/O	Z	LCD_DATA14(A/B) Sensor1_D6(A) PAP_D14(A/B) TS1_DATA2 SD0_CMD(D)
122	PB5	I/O	Z	LCD_DATA13(A/B) Sensor1_D5(A) PAP_D13(A/B) TS1_DATA1 SD0_DATA0(D)
123	PB4	I/O	Z	LCD_DATA12(A/B) Sensor1_D4(A) PAP_D12(A/B) TS1_DATA0 SD0_DATA1(D)
124	PB3	I/O	Z	LCD_DATA11(A/B) Sensor1_D3(A) PAP_D11(A/B) TS1_SYNC SD0_DATA2(D)
125	PB2	I/O	Z	LCD_DATA10(A/B) Sensor1_D2(A) PAP_D10(A/B) TS1_CLK SD0_DATA3(D)
126	PB1	I/O	Z	LCD_DATA9(A/B) Sensor1_D1(A) PAP_D9(A/B) TS1_VALID
127	PB0	I/O	Z	LCD_DATA8(A/B) Sensor1_D0(A) PAP_D8(A/B) TS1_ERROR

Pin No.	Name	Type	IO Initial State	Description
128	PA15	I/O	Z	LCD_SYNC2(A/B) Sensor1_SYNC1(A)
129	PA14	I/O	Z	LCD_SYNC1(A/B) Sensor1_SYNC0(A) PAP_RD(A/B)
130	PA13	I/O	Z	LCD_DCLK(A/B) Sensor1_CLK(A) TS0_DATA7
131	PA12	I/O	Z	LCD_SYNC0(A/B) PAP_WR(A/B) TS0_DATA6
132	DVDD	P	--	Digital Logic Power

Note

1.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.

2.Timer, CAN, MCPWM, QDEC, UART, LEDC, I²C, I²S and SPI functions can be remapped to any I/O (except PF/PR/PV/CSI/DSI).

Table 2-2-2 Pin Types Description

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
RF	RF antenna	O	Output

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-20	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
IOVDD		-0.3	3.6	V
IOVDD2		-0.3	3.6	V
IOVDD3		-0.3	3.6	V
RTCVD33		-0.3	3.6	V
DCVDD		-0.3	1.54	V
WVDD33		-0.3	3.6	V
WVDD14		-0.3	1.54	V
USBAVDD		-0.3	3.6	V
AVD33		-0.3	3.6	V
AVD12		-0.3	1.54	V
GPIO	Input voltage of GPIO (except PD2/PD3/PD4/PD5)	-0.3	3.6	V
HVTIO	Input voltage of HVT-IO (PD2/PD3/PD4/PD5)	-0.3	5.5	V

Note

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±300V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1kV	All pins	ANSI/ESDA/JEDEC JS-002-2022

3.3 PMU Characteristics

Table 3-3 PMU Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Power supply	--	2.7	3.7	5.5	V
Operating mode						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Voltage output	--	2.4	3.3	3.4	V
	Loading current	IOVDD=3.3V@VBAT = 3.9V	--	--	200	mA
AVDD28	Voltage output	--	2.5	2.8	3.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Loading current	AVDD28=2.8V@IOVDD = 3.3V	--	--	100	mA
AVDD18	Voltage output	--	1.5	1.8	2.2	V
	Loading current	AVDD18=1.8V@IOVDD = 3.3V	--	--	60	mA
DCVDD	Voltage output	--	--	1.4	--	V
	Loading current	DCVDD=1.4V@IOVDD = 3.3V, LDO mode	--	--	60	mA
		DCVDD=1.4V@VBAT = 3.7V, DCDC mode	--	--	180	mA
Low Power mode						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Loading current	IOVDD=3.0V@VBAT = 3.7V	--	--	10	mA

3.4 IO Characteristics

Table 3-4 IO Characteristics

Input Characteristics						
Symbol	Parameter	Conditions	IO	Min	Max	Unit
V _{IL}	Low-Level Input Voltage	IOVDD3 = 3.0V	PA1~PA11	-0.3	1.4	V
		IOVDD3 = 1.8V	PA1~PA11	-0.3	0.7	V
		IOVDD2 = 3.0V	PE10~PE15	-0.3	1.4	V
		IOVDD2 = 1.8V	PE10~PE15	-0.3	0.7	V
		IOVDD = 3.0V	PA12~PA15 PB0~PB15 PC0~PC13 PD0~PD1 PD6~PD15 PE0~PE9 PF0~PF5 FUSBDP FUSBDM HUSBDP HUSBDM PR0~PR1 PV0~PV1	-0.3	1.4	V
			PD2~PD5	-0.3	1.0	V
			IOVDD3 = 3.0V	1.7	3.3	V
			IOVDD3 = 1.8V	1.1	2.0	V
			IOVDD2 = 3.0V	1.7	3.3	V
			IOVDD2 = 1.8V	1.1	2.0	V
			PA12~PA15 PB0~PB15 PC0~PC13 PD0~PD1	1.7	3.3	V
V _{IH}	High-Level Input Voltage	IOVDD3 = 3.0V	PA1~PA11	1.7	3.3	V
		IOVDD3 = 1.8V	PA1~PA11	1.1	2.0	V
		IOVDD2 = 3.0V	PE10~PE15	1.7	3.3	V
		IOVDD2 = 1.8V	PE10~PE15	1.1	2.0	V
		IOVDD = 3.0V	PA12~PA15 PB0~PB15 PC0~PC13 PD0~PD1	1.7	3.3	V

			PD6~PD15 PE0~PE9 PF0~PF5 FUSBDP FUSBDM HUSBDP HUSBDM PR0~PR1 PV0~PV1			
		IOVDD = 3.0V	PD2~PD5	1.2	5.5	V
Output Characteristics						
Symbol	Parameter	Conditions	IO	Typ	Unit	
I _{OL}	Output Current	IOVDD3 = 3.0V Voutput = 0.3V	PA1~PA11	2.5(HD=0) 8(HD=1) 18.5(HD=2) 24(HD=3)	mA	
		IOVDD3 = 1.8V Voutput = 0.2V				
		IOVDD2 = 3.0V Voutput = 0.3V	PE10~PE15	2.5(HD=0) 8(HD=1) 18.5(HD=2) 24(HD=3)	mA	
		IOVDD2 = 1.8V Voutput = 0.2V				
		IOVDD = 3.0V Voutput = 0.3V	PA12~PA15 PB0~PB15 PC0~PC13 PD0~PD1 PD6~PD15 PE0~PE9 PF0~PF5	2.5(HD=0) 8(HD=1) 18.5(HD=2) 24(HD=3)	mA	
			PR0~PR1 PV0~PV1	2.5(HD=0) 18.5(HD=1)	mA	
			FUSBDP FUSBDM HUSBDP HUSBDM PD2~PD5	8	mA	
I _{OH}	Output Current	IOVDD3 = 3.0V Voutput = 2.7V	PA1~PA11	2.5(HD=0) 8(HD=1) 18.5(HD=2) 24(HD=3)	mA	
		IOVDD3 = 1.8V Voutput = 1.6V				
		IOVDD2 = 3.0V Voutput = 2.7V	PE10~PE15	2.5(HD=0) 8(HD=1)	mA	

		IOVDD2 = 1.8V Voutput = 1.6V		18.5(HD=2) 24(HD=3)	
		IOVDD = 3.0V Voutput = 2.7V	PA12~PA15 PB0~PB15 PC0~PC13 PD0~PD1 PD6~PD15 PE0~PE9 PF0~PF5	2.5(HD=0) 8(HD=1) 18.5(HD=2) 24(HD=3)	mA
			PR0~PR1 PV0~PV1	2.5(HD=0) 18.5(HD=1)	mA
			FUSBDP FUSBDM HUSBDP HUSBDM PD2~PD5	8	mA
Internal Resistance Characteristics					
Symbol	Parameter	Conditions	IO	Typ	Unit
R _{pu}	Pull-up Resistance	IOVDD = 3.0V IOVDD2 = 3.0V/1.8V IOVDD3 = 3.0V/1.8V	PA1~PA15 PB0~PB15 PC0~PC13 PD0~PD1 PD6~PD15 PE0~PE15 PF0~PF5	10k	Ω
			HUSBDP	1.5k(PU=1) 1k(PU=2/3)	Ω
			FUSBDP	1.5k	Ω
			FUSBDM	180k	Ω
R _{pd}	Pull-down Resistance	IOVDD = 3.0V IOVDD2 = 3.0V/1.8V IOVDD3 = 3.0V/1.8V	PA1~PA15 PB0~PB15 PC0~PC13 PD0~PD1 PD6~PD15 PE0~PE15 PF0~PF5	10k	Ω
			HUSBDP HUSBDM FUSBDP FUSBDM	15k	Ω

Note**1.Internal pull-up/pull-down resistance accuracy ±20%.**

3.5 Audio DAC Characteristics

Table 3-5 Stereo DAC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bits
Output Sample Rate	--	8	--	96	kHz
SNR	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	103	--	dB
	Single Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	100	--	dB
Dynamic Range	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	103	--	dB
	Single Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	100	--	dB
THD+N	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	-87	--	dB
	Single Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	-75	--	dB
Noise Floor	Differential Mode B/W=20Hz~20kHz A-Weighted load=10kΩ	--	6.4	--	uVrms
	Single Mode B/W=20Hz~20kHz A-Weighted load=10kΩ	--	5.4	--	uVrms

3.6 Audio ADC Characteristics

Table 3-6 Audio ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bits
Input Sample Rate	--	8	--	48	kHz
SNR	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	95	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	92	--	dB
Dynamic Range	Differential input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	95	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	92	--	dB
THD+N	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-87	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-81	--	dB
Analogue Gain		-6	--	28	dB
Max Input Level	Differential input Mode ADC gain=0dB	--	0.7	--	Vrms
	Single-ended input Mode ADC gain=0dB	--	0.35	--	Vrms

3.7 BT Characteristics

3.7.1 Transmitter

Table 3-7-1 Transmitter characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Maximum RF Transmit Power	BR	--	19	--	dBm
Maximum RF Transmit Power	EDR $\pi/4$ DQPSK EDR 8DPSK	--	19	--	dBm
Relative Transmit Power	EDR $\pi/4$ DQPSK EDR 8DPSK	--	1.5	--	dB
Maximum RF Transmit Power	BLE-1Mbps	--	19	--	dBm

3.7.2 Receiver

Table 3-7-2 Receiver characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity	BR	--	-95.5	--	dBm
	EDR $\pi/4$ DQPSK	--	-96	--	dBm
	EDR 8DPSK	--	-88	--	dBm
	BLE-1Mbps	--	-98	--	dBm
	BLE-2Mbps	--	-95	--	dBm
	BLE-S2	--	-101	--	dBm
	BLE-S8	--	-106	--	dBm

3.8 WiFi Characteristics

3.8.1 Transmitter

TX Power with Spectral Mask and EVM Meeting 802.11 Standards.

Table 3-8-1 Transmitter characteristics

Parameter	Conditions	Min	Typ	Max	Unit
TX Power	802.11b, 1 Mbps, DSSS	--	19	--	dBm
	802.11b, 11 Mbps, CCK	--	19	--	dBm
	802.11g, 6 Mbps, OFDM	--	17	--	dBm
	802.11g, 54 Mbps, OFDM	--	14	--	dBm
	802.11n, HT20, MCS0	--	17	--	dBm
	802.11n, HT20, MCS7	--	13	--	dBm
	802.11n, HT40, MCS0	--	17	--	dBm
	802.11n, HT40, MCS7	--	12	--	dBm

3.8.2 Receiver

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n.

Table 3-8-2 Receiver characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity	802.11b, 1 Mbps, DSSS	--	-97	--	dBm
	802.11b, 2 Mbps, DSSS	--	-94.5	--	dBm
	802.11b, 5.5 Mbps, CCK	--	-93	--	dBm
	802.11b, 11 Mbps, CCK	--	-90	--	dBm
	802.11g, 6 Mbps, OFDM	--	-93	--	dBm
	802.11g, 9 Mbps, OFDM	--	-92	--	dBm
	802.11g, 12 Mbps, OFDM	--	-91	--	dBm
	802.11g, 18 Mbps, OFDM	--	-89	--	dBm
	802.11g, 24 Mbps, OFDM	--	-86	--	dBm
	802.11g, 36 Mbps, OFDM	--	-83	--	dBm
	802.11g, 48 Mbps, OFDM	--	-79	--	dBm
	802.11g, 54 Mbps, OFDM	--	-77	--	dBm
	802.11n, HT20, MCS0	--	-93	--	dBm
	802.11n, HT20, MCS1	--	-90.5	--	dBm
	802.11n, HT20, MCS2	--	-88	--	dBm
	802.11n, HT20, MCS3	--	-84.5	--	dBm
	802.11n, HT20, MCS4	--	-81.5	--	dBm
	802.11n, HT20, MCS5	--	-77	--	dBm
	802.11n, HT20, MCS6	--	-75	--	dBm
	802.11n, HT20, MCS7	--	-74	--	dBm
	802.11n, HT40, MCS0	--	-89	--	dBm
	802.11n, HT40, MCS1	--	-86	--	dBm
	802.11n, HT40, MCS2	--	-84	--	dBm
	802.11n, HT40, MCS3	--	-80	--	dBm
	802.11n, HT40, MCS4	--	-77.5	--	dBm
	802.11n, HT40, MCS5	--	-72.5	--	dBm
	802.11n, HT40, MCS6	--	-71.5	--	dBm
	802.11n, HT40, MCS7	--	-70	--	dBm
	802.11n, HT40, MCS32	--	-89	--	dBm

4 Package Information

4.1 QFN132_10*10mm

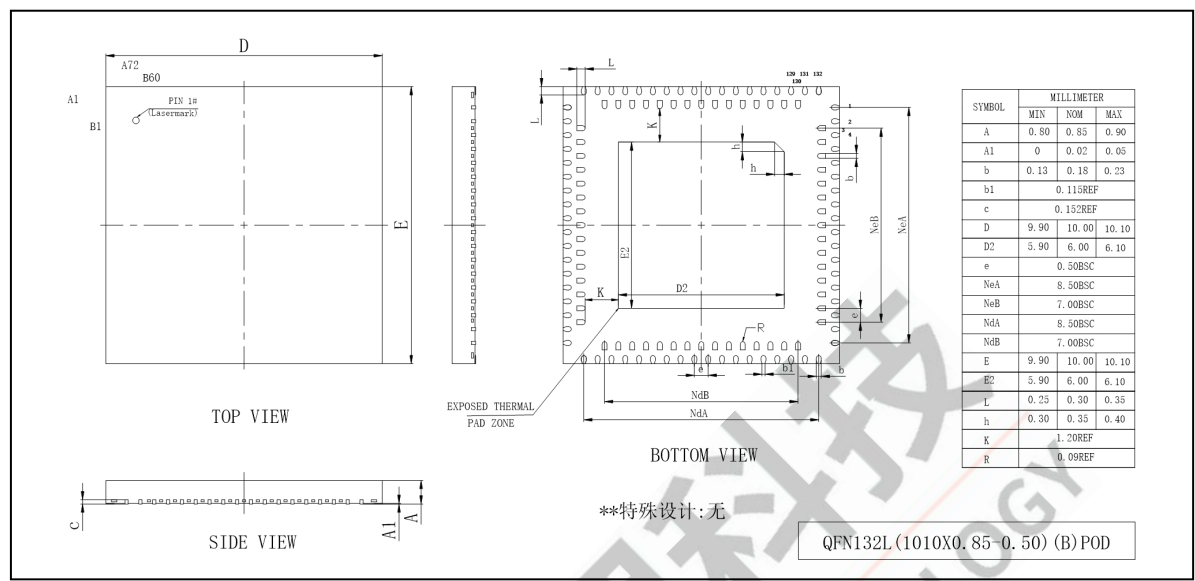


Figure 4-1 AC7926A Package

5 IC Marking Information

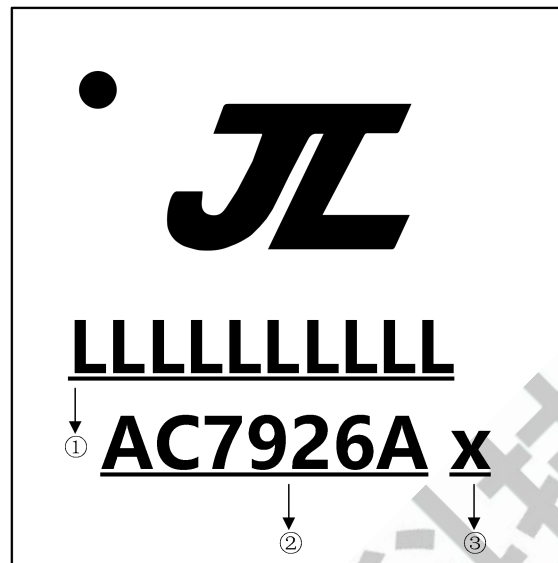


Figure 5-1 AC7926A Package Outline

- ① Production Batch
- ② Chip Model
- ③ Built-in DDR size
 - 0 No Flash Memory
 - 2 2Mbit flash
 - 4 4Mbit flash
 - 8 8Mbit flash
 - 6 16Mbit flash
 - 3 32Mbit flash
 - 5 64Mbit flash
 - 7 128Mbit flash
 - A 1Mx16 SDRAM
 - B 4Mx16 SDRAM
 - E 4Mx16bit DDR1
 - F 8Mx16bit DDR1
 - G 16Mx16bit DDR1

6 Solder-Reflow Condition

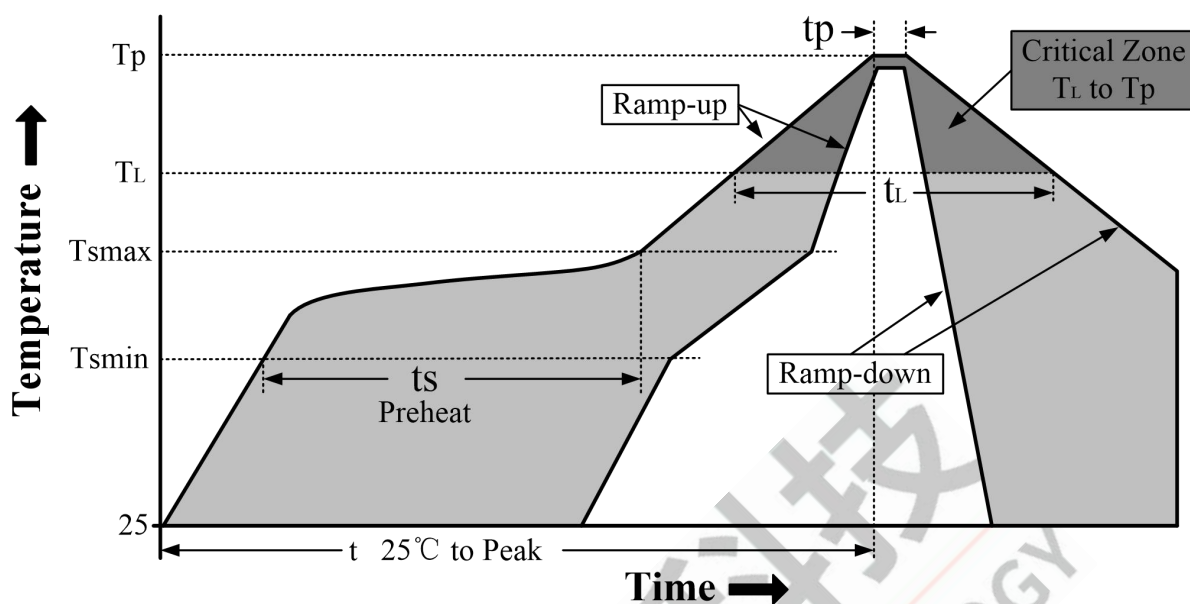


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100°C	150°C
	Temperature Max (T_{smax})	150°C	200°C
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3°C/second max	3°C/second max
Liquidous temperature (T_L)		183°C	217°C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5°C of actual Peak Temperature (tp) ²		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

Note

- 1.All temperatures refer to topside of the package, measured on the package body surface
- 2.Time within 5°C of actual peak temperature (tp) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 6-3 Pb-free - Classification Temperature

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6mm	260°C	260°C	260°C
1.6 mm - 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

Note

1.*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.