

JL6976M Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 1.2

Date: 2024.08.16

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

JL6976M Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64 Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC, AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR >= 101dB
- Two channels 24-bit ADC, SNR >= 92dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- Two analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- One channel Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth

V5.4+BR+EDR+BLE specification

(QDID: 223418)

- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides a maximum +8dbm transmitting power
- receiver with minimum -94dBm sensitivity
- Fast AGC for enhanced dynamic range
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile A2DP 1.4\AVCTP 1.4\AVDTP 1.3\AVRCP 1.6.2\HFP 1.8\SPP 1.2\RFCOMM 1.2\PNP 1.3\HID 1.1.1\SDP core5.4\L2CAP core 5.4

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- One hard ware IIC interface supports host and device mode
- Built-in Cap Sense Key controller
- Two Built-in low power Cap Sense Keys
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- VDDIO is 2.2V to 3.4V

Packages

● QFN32(4mm*4mm)

● Storage temperature: -65℃ to +150℃

Temperature

● Operating temperature: -40℃ to +85℃

Applications

● 2.4G wireless MIC

● Game Earphone



1、 Pin Definition

1.1 Pin Assignment

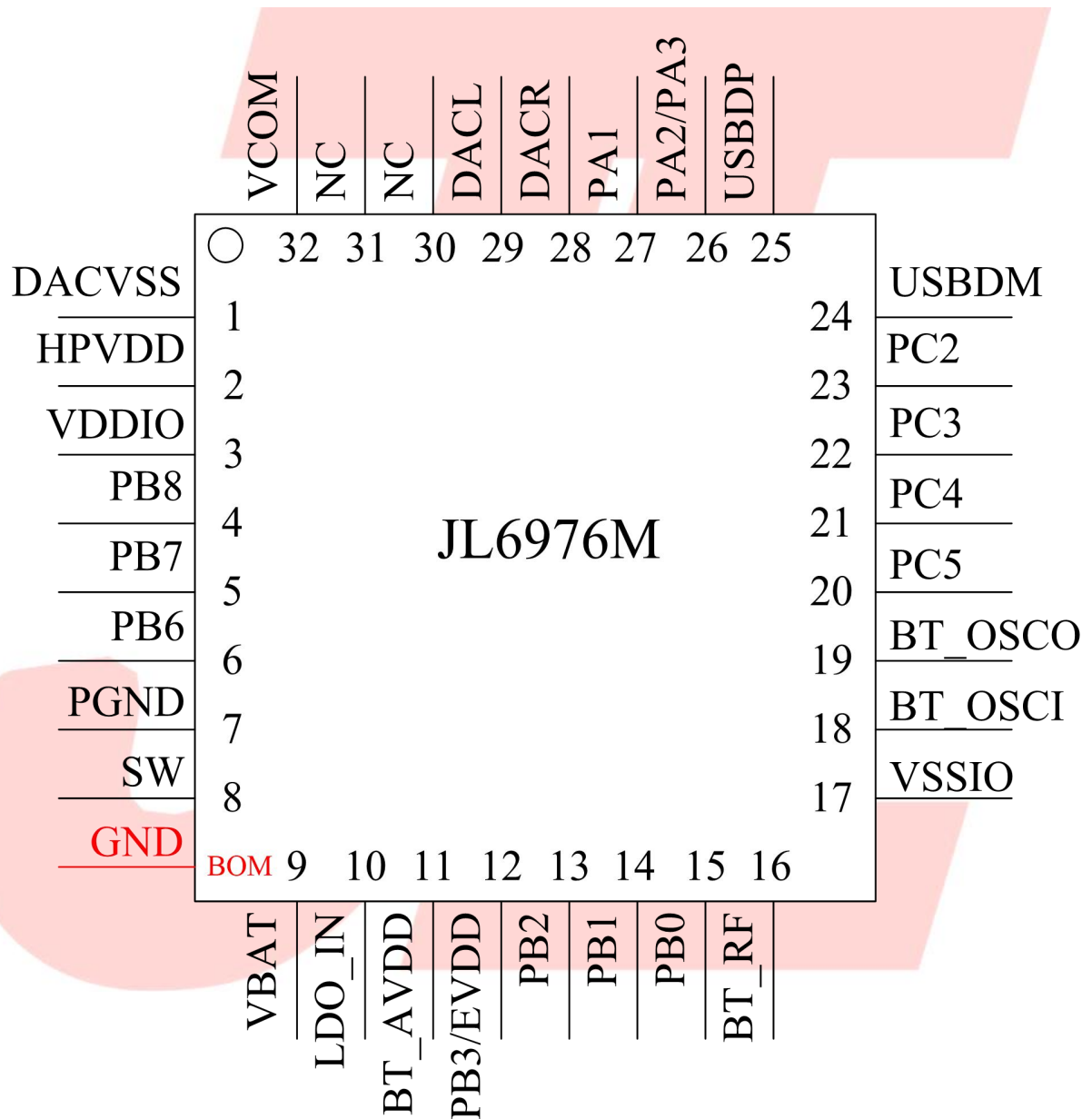


Figure 1-1 JL6976M Package Diagram

1.2 Pin Description

Table 1-1 JL6976M Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	DACVSS	P	/		Analog Ground
2	HPVDD	P	/		Headphone AMP Power
3	VDDIO	P	/		IO Power 3.3v
4	PB8	I/O	8/24	GPIO	MIC1: MIC1 Input Channel; UART0RXB: Uart0 Data Input(B); CAP4: Timer4 Capture;
5	PB7	I/O	8/24	GPIO	MIC_BIAS1: MIC1 Bias Output; UART0TXB: Uart0 Data Output(B);
6	PB6	I/O	8/24	GPIO	UART1RXA: Uart1 Data Input(A); PWM2: Timer2 PWM Output; ADC9: ADC Input Channel 9; Touch7: Touch Input Channel 7;
7	PGND	P	/		DCDC Ground
8	SW	P	/		DCDC switch output, connected to inductor
9	VBAT	P	/		Power Supply, connect to battery
10	LDO_IN	P	/		Charge Power Input; UART0TXC: Uart0 Data Output(C); UART0RXC: Uart0 Data Input(C); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
11	BT_AVDD	P	/	GPIO	BT Power
12	PB3	I/O	8/24	GPIO	
	EVDD	P	/		EVDD: Supply volte to peripherals
13	PB2	I/O	8/24	GPIO	UART2RXC: Uart2 Data Input(C); SPI2DOC: SPI2 Data Out(C); CAP5: Timer5 Capture; ADC7: ADC Input Channel 7; LP_TH1: Low Power Touch Channel 1
14	PB1	I/O	8/24	GPIO (pull up)	Long Press Reset; SPI2CLKC: SPI2 Clk(C); UART2TXC: Uart2 Data Output(C) ADC6: ADC Input Channel 6; LP_TH0: Low Power Touch Channel 0

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

15	PB0	I/O	8	GPIO (High Voltage Input)	SPI2_DIC: SPI2 Data In(C); ALNK_MCLK(B): ALNK1 Master Clock(B); TMR4: Timer4 Clock Input;
16	BT_RF	/	/		BT Antenna
17	VSSIO	P	/		Ground
18	BT_OSCI	I	/		BTOSC In
19	BT_OSCO	O	/		BTOSC Out
20	PC5	I/O	8/24	GPIO	UART2RXD: Uart2 Data Input(D); SPI1DOB: SPI1 Data Out(B); ALNK_DAT3(B): Audio Link Data3(B); IIC_SDA_B: IIC SDA(B); ADC5: ADC Input Channel 5;
21	PC4	I/O	8/24	GPIO	UART2TXD: Uart2 Data Output(D); SPI1CLKB: SPI1 Clock(B); ALNK_DAT2(B): Audio Link Data2(B); IIC_SCL_B: IIC SCL(B); ADC4: ADC Input Channel 4; PWM4: Timer4 PWM Output;
22	PC3	I/O	8/24	GPIO	UART0RXD: Uart0 Data Input(D); SPI1DIB: SPI1 Data In(B); ALNK_LRCK(B): Audio Link Word Select(B); IIC_SDA_C: IIC SDA(C); TMR3: Timer3 Clock Input;
23	PC2	I/O	8/24	GPIO	ALNK_SCLK(B): Audio Link Serial Clock(B); IIC_SCL_C: IIC SCL(C); UART0TXD: Uart0 Data Output(D); TMR1: Timer1 Clock Input;
24	USBDM	I/O	4	USB Negative Data	UART1RXD: Uart1 Data Input(D); IIC_SDA_A: IIC SDA(A); ADC11: ADC Input Channel 11;
25	USBDP	I/O	4	USB Positive Data	UART1TXD: Uart1 Data Output(D); IIC_SCL_A: IIC SCL(A); ADC10: ADC Input Channel 10;
26	PA3	I/O	8/24	GPIO	UART2TXA: Uart2 Data Output(A); ADC0: ADC Input Channel 0; PWM1: Timer1 PWM Output; Touch0: Touch Input Channel 0;
	PA2	I/O	8/24	GPIO	ALNK_MCLK(A): ALNK Master Clock(A); MIC_BIAS0: MIC0 Bias Output; MIC0_N: Different MIC0 Negative CAP3: Timer3 Capture;

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

					UART1RXC: Uart1 Data In(C);
27	PA1	I/O	8/24	GPIO	MIC0: MIC0 Input Channel ; PWM0: Timer0 PWM Output; UART1TXC: Uart1 Data Output(C);
28	DACR	O	/		DAC Right Channel
29	DACL	O	/		DAC Left Channel
30	NC				
31	NC				
32	VCOM	P	/		DAC reference voltage

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
LDO_IN	Charger Voltage	-0.3	6	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.2	V	
LDO_IN	Charger supply Voltage	4.5	5.0	5.5	V	
Normal mode						
VDDIO	Voltage output	—	3.0	—	V	VBAT = 4.2V, 10mA loading
	Loading current	—	—	100	mA	VDDIO=3V@VBAT = 4.2V
BT_AVDD	Voltage output	—	1.3	—	V	VDDIO=3.0V, 10mA loading
	Loading current	—	—	60	mA	BT_AVDD=1.25V@VDDIO=3.0v
EVDD	Voltage output	—	1.1	—	V	BT_AVDD=1.25V, 1mA loading
	Loading current	—	—	5	mA	EVDD=1.1V@BT_AVDD=1.25v
LP mode						
VDDIO	Loading current			5	mA	VDDIO=3V@VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	—
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	LDO_IN>4.5V

		4.30	4.35	4.40	V	LDO_IN > 4.65V
I _{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I _{Trickl}	Trickle Charge Current	20	45	70	mA	V _{BAT} < V _{Trickl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* VDDIO	V	VDDIO = 3.3V
V _{IH}	High-Level Input Voltage	0.7* VDDIO	—	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	—	—	0.33	V	VDDIO = 3.3V
V _{OH}	High-Level Output Voltage	2.7	—	—	V	VDDIO = 3.3V

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1~PA3 PC2~PC5 PB3~PB3 PB6~PB8	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy ±20%
PB0	8mA	—	10K	10K	
USBDP	4mA	—	1.5K	15K	
USBDM	4mA	—	180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	—	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	—	-80	—	dB	
S/N	—	101	—	dB	
Crosstalk	—	-80	—	dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

Output Swing		0.45		Vrms	
Dynamic Range		90		dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	—	20	30	mW	16ohm loading

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		92		dB	Fsample=44.1kHz Fin=1KHz 2mVpp Input
S/N	—	92	—	dB	Fsample=44.1kHz Fin=1KHz 1.2Vpp Input
THD+N	—	-75	—	dB	
Crosstalk	—	-80	—	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		6	8	dBm	25°C, Power Supply VBAT=5V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1		dB	25°C, Power Supply VBAT=5V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
Transmit Power	-2MHz	-38		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

2.8.2 Receiver

Basic Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

2.8.3 BLE Transmitter

1M Data Rate

Table 2-12

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
RF Transmit Power			7	9	dB	
In-band Spurious Emission	+2MHz		-42	-20	dB	
	-2MHz		-34	-20	dB	
	+3MHz		-46	-30	dB	
	-3MHz		-36	-30	dB	
Modulation	$\Delta f_{l\text{ avg}}$	225	247			

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

	Δf_2 99%	185	236			
	$\Delta f_{1avg}/\Delta f_{2av}$	0.8	0.9			
Carrier Frequency Offset		-150	+/-10	+150	KHz	
Frequency Drift		-50	+/-5	+50	KHz	
Frequency Drift Rate		-20	3	+20	KHz/50us	

2M Data Rate**Table 2-13**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	
RF Transmit Power			7	9	dB	
Adjacent Channel Transmit	+2MHz		-46	-20	dB	25°C, Power Supply VBAT=5V 2441MHz
	-2MHz		-38	-20	dB	
	+3MHz		-53	-30	dB	
	-3MHz		-42	-30	dB	
Frequency Deviation	Δf_1 avg	450	520			
	Δf_2 99%	370	500			
	$\Delta f_{1avg}/\Delta f_{2av}$	0.8	0.9			
Carrier Frequency Offset		-150	+/-10	+150	KHz	
Frequency Drift		-50	+/-5	+50	KHz	
Frequency Drift Rate		-20	+/-3	+20	KHz/50us	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、Package Information

3.1 QFN32_4.0x4.0

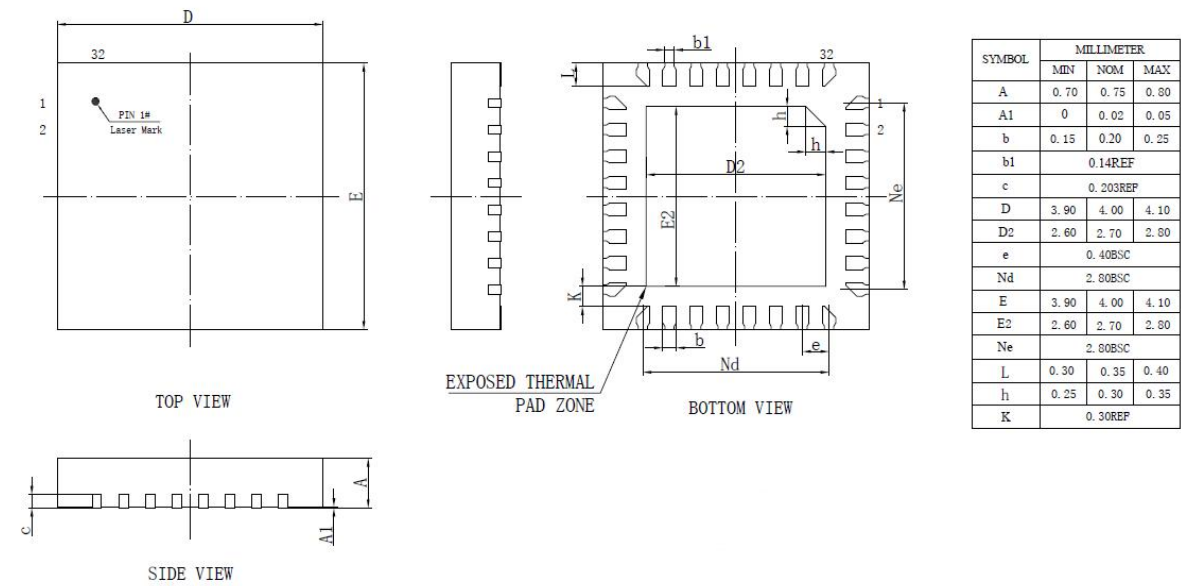


Figure 3-1 JL6976M Package

4、Revision History

Date	Revision	Description
2020.08.31	V1.0	Initial Release
2023.12.01	V1.1	Update JL6976M BT_Features
2024.08.16	V1.2	Update DAC Characteristics